Amendments to the Claims:

The listing of claims will replace all prior versions and listings of claims in the application:

Listing of Claims:

1. (Currently Amended) An apparatus for sampling timing compensation at a receiver of a communication system, wherein each of a first symbol and a second symbols comprises ~~comprising~~ at least two pilot signals, the pilot signals of each of the first and second symbols have a first part transmitted via a first pilot subchannel and a second part transmitted via a second pilot subchannels ~~respectively~~ and the first and the second pilot subchannels comprise a first and a second pilot indexes respectively, the apparatus comprising:

a pilot subchannel estimator for generating a first frequency response of each of the first and the second symbols respectively according to the first part of the pilot signals of each of the first and the second symbols transmitted over the first pilot subchannel and for generating a second frequency response of each of the first and second symbols respectively according to the second part of the pilot signals of each of the first and second symbols transmitted over the second pilot subchannel;

a timing offset estimator, coupled to the pilot subchannel estimator, for calculating a timing offset according to a first difference between the first frequency responses of the first and second symbols, a second difference between the second frequency responses of the first and second symbols and a difference between the first and second differences ~~frequency response~~; and

a phase rotator, coupled to the timing offset estimator, for performing sampling timing compensation according to an phase rotation corresponding to the timing offset.

2. (Original) The apparatus of claim 1, wherein the communication system is a

multi-carrier system.

3. (Currently Amended) The apparatus of claim 1, wherein the timing offset estimator further comprises a phase difference calculating device for calculating the first difference and the second difference ~~a phase difference between the first and second frequency responses~~, and a divider for calculating the timing offset according to the difference between the first and second differences and ~~the phase difference and a difference between~~ the first and the second pilot indexes.

4. (Cancelled)

5. (Withdrawn) The apparatus of claim 1, further comprises:

a timing controller for generating a control signal according to the timing offset; and

a cyclic prefix remover for removing a cyclic prefix of the symbol according to the control signal.

6. (Original) The apparatus of claim 1, further comprising:

a timing controller for generating a control signal according to the timing offset;

a clock generator for generating a sampling clock according to the control signal, wherein the phase of the sampling clock is adjusted according to the control signal; and

an analog-to-digital converter (ADC) for converting the symbol according to the sampling clock.

7. (Previously Presented) The apparatus of claim 6, wherein a period of the sampling clock (T_f) is shorter than a sampling interval (Ts) of the ADC.

8. (Previously Presented) The apparatus of claim 7, wherein the period of the sampling clock (T_f) is a fraction of the sampling interval (T_s) of the ADC.

9. (Original) The apparatus of claim 6, wherein the clock generator further comprises

a phase-locked loop (PLL) circuit.

10. (Currently Amended) A method for sampling timing compensation used at a receiver of a communication system, wherein each of a first symbol and a second symbol comprising at least two pilot signals, the pilot signals of each of the first and second symbols have a first part transmitted via a first pilot subchannel and a second part transmitted via a second pilot subchannels ~~respectively~~, and the first and the second pilot subchannels comprise a first and a second pilot indexes respectively, comprising:

generating a first frequency response of each of the first and the second symbols respectively according to the first part of the pilot signals of each of the first and the second symbols transmitted over the first pilot subchannel;

generating a second frequency response of each of the first and the second symbols respectively according to the second part of the pilot signals of each of the first and the second symbols transmitted over the second pilot subchannel;

generating a first difference between the first frequency responses of the first and second symbols;

generating a second difference between the second frequency responses of the first and second symbols;

calculating a timing offset according to a difference between the first and second differences ~~frequency response~~; and

performing sampling timing compensation according to a phase rotation corresponding to the timing offset.

11. (Cancelled)

12. (Currently Amended) The method of claim 10 [[11]], wherein the timing offset is calculated according to the ~~phase~~ difference between the first and second differences and ~~a difference between~~ the first and the second pilot indexes.

13. (Cancelled)

14. (Cancelled)

15. (Withdrawn) The method of claim 10, further comprising:

generating a control signal according to the timing offset; and

removing a cyclic prefix of the symbol according to the control signal.

16. (Previously Presented) The method of claim 10, further comprising:

generating a control signal according to the timing offset; and

generating a sampling clock according to the control signal, wherein a phase of the sampling clock is adjusted according to the control signal.

17. (Cancelled)

18. (Currently Amended) An apparatus for sampling timing compensation at a receiver of a communication system, wherein each of a first symbol and a second symbol comprising at least two pilot signals, the pilot signals of each of the first and second symbols have a first part transmitted via a first pilot subchannel and a second part transmitted via a second pilot subchannels ~~respectively,~~ and the first and the second pilot subchannels comprise a first and a second pilot indexes respectively, the apparatus comprising:

a pre-FFT processing device for processing the first and the second symbols in a time domain;

a FFT for transforming the first and the second symbols to a frequency domain;

a pilot subchannel estimator for generating a first frequency response of each of the first and the second symbols respectively according to the first part of the pilot signals of each of the first and the second symbols transmitted over the first pilot subchannel and for generating a second frequency response of each of the first and second symbols respectively according to the second part of the pilot

signals of each of the first and second symbols transmitted over the second pilot subchannel;

a timing offset estimator, coupled to the pilot subchannel estimator, for calculating a timing offset according to a first difference between the first frequency responses of the first and second symbols, a second difference between the second frequency responses of the first and second symbols and a difference between the first and second differences ~~frequency responses~~;

a phase rotator, coupled to the timing offset estimator, for performing sampling timing compensation according to an phase rotation corresponding to the timing offset; and

a adjusting device for adjusting the operation of the pre-FFT processing device.

19. (Original) The method of claim 18, wherein the pre-FFT processing device includes an ADC.

20. (Original) The method of claim 19, wherein the adjusting device includes:

a timing controller for generating a control signal according to the timing offset; and

a clock generator for generating a sampling clock according to the control signal for controlling the operation of the ADC, wherein the phase of the sampling clock is adjusted according to the control signal.

21. (Withdrawn) The method of claim 18, wherein the pre-FFT processing device includes a cyclic prefix remover.

22. (Withdrawn) The method of claim 21, wherein the adjusting device includes a timing controller for generating a control signal for controlling the operation of the cyclic prefix remover according to the timing offset.

23. (Currently Amended) An method for sampling timing compensation at a receiver of a communication system, wherein each of a first symbol and a second symbol

comprising at least two pilot signals, the pilot signals of each of the first and second symbols have a first part transmitted via a first subchannel and a second part transmitted via a second pilot subchannels ~~respectively,~~ and the first and the second pilot subchannels comprise a first and a second pilot indexes respectively, the method comprising:

processing the first and the second symbols in a time domain;

transforming the first and the second symbols to a frequency domain;

generating a first frequency response of each of the first and the second symbols respectively according to the first part of the pilot signals of each of the first and the second symbols transmitted over the first pilot subchannel and generating a second frequency response of each of the first and second symbols respectively according to the second part of the pilot signals of each of the first and second symbols transmitted over the second pilot subchannel;

generating a first difference between the first frequency responses of the first and second symbols;

generating a second difference between the second frequency responses of the first and second symbols;

calculating a timing offset according to a difference between the first and second differences ~~frequency responses~~;

performing sampling timing compensation according to an phase rotation corresponding to the timing offset; and

adjusting the operation of the step of processing symbols in the time domain.